WHAT IS CLAIMED IS:

1. A memory device comprising:

a gate member over a semiconductor;

a source region in the semiconductor;

a drain region in the semiconductor, said drain region having a depth shallower than said source region and not deeper than 0.1 μm;

a channel region being interposed between said source and drain regions and being adjacent to said gate member, and

wherein said source and drain regions extend from a surface of said semiconductor to said depth not longer than a thickness of said semiconductor,

wherein said source region overlaps with said gate member,

wherein said channel region has a length not longer than 0.3 μm.

2. A device according to claim 1, wherein said semiconductor is crystal silicon.

3. A memory device comprising:

a gate electrode having a floating gate, a control gate and an oxide on a semiconductor substrate, said oxide being provided on surfaces of the floating gate and the control gate;

a source region in the semiconductor;

a drain region in the semiconductor, said drain region having a depth shallower than said source region and not deeper than 0.1 μm; and

a channel region being interposed between said source and drain regions being adjacent to said gate electrode,

wherein said source region overlaps with said gate electrode,

wherein said channel region has a length not longer than 0.3 μm.

4. A device according to claim 3, wherein said semiconductor substrate is a crystal silicon substrate.

5. A memory device comprising:

a semiconductor substrate;

a first silicon film introduced with an n-type impurity over said semiconductor substrate;

a second silicon film introduced with an n-type impurity over said first silicon film;

an insulating film interposed between said semiconductor substrate and said first silicon film and between said first and second silicon film;

a first impurity region formed in the semiconductor substrate, said first impurity region overlapping with said insulating film;

a second impurity region formed in the semiconductor substrate, said second impurity region being not contact with said first impurity region and having a depth shallower than said first impurity region and not deeper than 0.1 μm;

a channel region formed between said first and second impurity region,

wherein said channel region has a length not longer than 0.3 μm.

6. A device according to claim 5, wherein said semiconductor substrate is a crystal silicon substrate.

7. A memory device comprising:

a semiconductor substrate;

at least two gate electrodes over said semiconductor substrate;

a first impurity region formed between said gate electrodes;

at least two second impurity regions formed adjacent to said gate electrodes, each of said second impurity region having a depth shallower than that of said first impurity region; and

at least two channel regions in the semiconductor substrate, each of said channel regions being formed between said first impurity region and each of second impurity regions, and being adjacent to each of said gate electrodes,

wherein said depth of each of said second impurity regions is not deeper than 0.1 μm,

wherein said first impurity region overlaps with each of said gate electrodes,

wherein each of said channel regions has a length not longer than 0.3 μm.

8. A device according to claim 7, wherein said semiconductor substrate is a crystal silicon substrate.

9. A memory device comprising:

a semiconductor substrate;

at least two gate electrodes over said semiconductor substrate, each of said gate electrodes having a floating gate, a control gate and an

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oxide on said semiconductor substrate, said oxide being provided on surfaces of the floating gate and the control gate;

a first impurity region formed between said gate electrodes;

at least two second impurity regions formed in adjacent with said gate electrodes, each of said second impurity region having a depth shallower than that of said first impurity region; and

at least two channel regions in the semiconductor substrate, each of said channel regions being formed between said first impurity region and each of second impurity regions,

wherein said depth of each of said second impurity regions is not deeper than 0.1 μm,

wherein said first impurity region overlaps with each of said gate electrodes,

wherein each of said channel regions has a length not longer than 0.3 μm.

10. A device according to claim 9, wherein said semiconductor substrate is a crystal silicon substrate.

11. A transistor comprising:

a pair of first impurity regions, each comprising an impurity at a first concentration;

a pair of second impurity regions, each being adjacent to the first impurity regions and comprising the impurity at a second concentration which is lower than the first concentration;

a channel region formed between the pair of second impurity regions;

a gate electrode at least adjacent to the channel region having a gate insulating film therebetween,

wherein said channel region has a length not longer than 0.3 μm.

12. A transistor comprising according to claim 11, wherein each of the second impurity regions has a depth not deeper 50 μm.

13. A transistor comprising:

a source region and a drain region, each of the source region and the drain region comprising an impurity at a first concentration;

a pair of LDD regions, each being adjacent to the source region and the drain region and comprising the impurity at a second concentration which is lower than the first concentration;

a channel region formed between the pair of LDD regions;

a gate electrode at least adjacent to the channel region having a gate insulating film therebetween,

wherein said channel region has a length not longer than 0.3 μm.

14. A transistor comprising according to claim 13, wherein each of the LDD regions has a depth not deeper 50 μm.

15. A MOS field effect transistor comprising:

a pair of n^+ impurity regions, each comprising an impurity at a first concentration;

a pair of n^- impurity regions, each being adjacent to the n^+ impurity regions and comprising the impurity at a second concentration which is lower than the first concentration;

a channel region formed between the pair of n^- impurity regions;

a gate electrode at least adjacent to the channel region having a gate insulating film therebetween,

wherein said channel region has a length not longer than 0.3 μm.

16. A transistor comprising according to claim 11, wherein each of the n^- impurity regions has a depth not deeper 50 μm.